IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	§	
Michael I. Catherwood	§	Group Art Unit: **2193**
	§	
Serial No.: **09/870,944**	§	
	§	Examiner: **Do, Chat C.**
Filed: **June 1, 2001**	§	
	§	
Title: **"DUAL MODE ARITHMETIC SATURATION PROCESSING"**	§	Atty. Docket No.: **068354.1443**

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

The following Pre- Appeal Brief Request for Review ("Request") is being filed in accordance with the provisions set forth in the Official Gazette Notice of July 12, 2005 ("OG Notice"). Pursuant to the OG Notice, this Request is being filed concurrently with a Notice of Appeal. The Applicants respectfully request reconsideration of the Application in light of the remarks set forth below.

REMARKS

Applicant contents that rejection of claims 1 and 3-5 contain clear legal and factual deficiencies, as described below. In a Final Office Action dated April 11, 2006, the Examiner rejected claims 1 and 3-5 under 35 U.S.C. § 102(b) as unpatentable over U.S. Patent No. 4,945,507 to Ishida et al. ("Ishida").

Claim 1 requires, in part, a system comprising "an accumulator, operatively connected to store at least a portion of the result of the added operands or at least a portion of a selected one of pre-determined constants based on control signals," "guard bits, operatively connected to store the remaining portion of the result of the added operands or the remaining portion of the selected one of predetermined constants based on the control signals," and "logic means for comparing most significant bits of the guard bits and most significant bits of the result of the added operands, and for generating the control signals in accordance with the comparison."

Ishida discusses an overflow correction circuit for use in an arithmetic operation circuit. Specifically, Ishida discloses an adder 10 whose output 22 can be detected for an overflow condition by detector 34. Depending upon the type of overflow condition, overflow detector 34 then directs the selector to forward one of three values (the maximum value 28, the minimum value 32 or the results of the adder 10) to the accumulator 46.

Ishida does not disclose each element of claim 1. For example, Ishida fails to teach a system for overflow and saturation processing comprising "**guard bits**, operatively connected to store **the remaining portion** of the result of the added operands or **the remaining portion** of the selected one of predetermined constants based on the control signals," as required

by Claim 1. (emphasis added) Ishida discusses a method and system for detecting and correcting overflow in an arithmetic circuit (see Abstract) but does not store the result of the overflow. The present invention contemplates, *inter alia*, not only detection of overflow (e.g. overflow logic), but also storing of the overflow (e.g. guard bits), and detecting whether such overflow itself overflows (e.g. saturation logic).

The Final Office Action states that Ishida's D22 and D23 in Figure 2 disclose the "guard bits" of claim 1. (Final Office Action at 2-3) The Response to Arguments portion of the Final Office states that "Generally, the most significant bit(s) of adder 10 are considered as the guard bit(s), which is stored in flip-flop register 62 in Figure 2 or 6." (Final Office Action at 4) First, Applicant notes that claim 1 requires "guard bits" and objects to the Office Action's characterization of this element as "guard bit(s)." The plurality of the guard bits is a limitation and cannot be read out of the claim. Applicant notes that there is only a single flip-flop register shown in each of Figures 2 and 6. With only a single register, the circuits can only store a single bit. Therefore Ishida's circuit in Figures 2 and 6 circuits do not disclose "guard bits . . . to store the remaining portion of the result," as required by the claim. Applicant further incorporates the detailed arguments made with respect to this claim element in Applicant's Response to Final Office Action at pages 5-6.

The mapping of Ishida to claim 1 becomes more strained when considering the limitation of "logic means for comparing **most significant bits of the guard bits and most significant bits of the result of the added operands**, and for generating the control signals in accordance with the comparison." The Final Office Action states that this limitation is also met by the circuit in Figure 2 and particularly by exclusive OR gate 66. (Final Office Action at 3) The inputs to the exclusive OR gate 66 are D22 and D23, which the Final Office Action earlier

characterizes as the "guard bits." (Final Office Action at 2-3) The Final Office Action does not explain how the two-input exclusive OR gate 66 compares the most significant bits of the guard bits and most significant bits of the result of the added operands. The Final Office Action's mapping of these two sets of "most significant bits" reads at least one of them out of the claim by attempting to show that they are disclosed by the same element in Ishida. The rejection, therefore, is improper and fails to disclose this element. Applicant further incorporates the detailed arguments made with respect to this claim element in Applicant's Response to Final Office Action at pages 6-7.

For at least these reasons, Ishida does not disclose each element of claim 1. Claims 3-5 depend from claim 1 and are similarly patentable over Ishida.

CONCLUSION

As the rejection of claims 1 and 3-5 contain clear deficiencies, Applicant respectfully requests a finding of allowance of claims 1 and 3-5. To the extent necessary, the Commissioner is authorized to charge any required fees or credit any overpayments to Baker Botts L.L.P. **Deposit Account No. 02-0383**, *(formerly Baker & Botts, L.L.P.)* **Order Number 068354.1443**.

Respectfully submitted,

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